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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,756	01/14/2004	Hajime Kimura	12732-0207001	1526

26171 7590 05/05/2010

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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
05/05/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/756,756	KIMURA ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,12,81 and 92-96* is/are pending in the application.

4a) Of the above claim(s) *95 and 96* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,12,81 and 92-94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

2. Newly submitted *claims 95 and 96* are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

I. ***Original Claims 11, 12, 81, and 92-94***, drawn to a signal line driver subcombination, classified in class *323*, subclass *315 (i.e., self-regulating circuits)*.

II. ***Newly Submitted Claims 95 and 96***, drawn to a display device combination, classified in class *345*, subclass *692 (i.e., display driving control circuitry)*.

The inventions are distinct, each from the other because of the following reasons:

Inventions ***II*** and ***I*** are related respectively as combination and subcombination.

Inventions in this relationship are distinct if it can be shown that:

(1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and

(2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)).

(1) In the instant case, the ***Combination*** (*in claims 95 and 96*) as claimed does not require the particulars of the ***Subcombination*** as claimed (*in claims 11, 12, 81, and 92-94*) because:

The ***Combination*** as claimed (*in claims 95 and 96*) does not require:

"*a shift register*," as claimed in independent claim 11 (*line 2*);

"*a latch circuit, electrically connected to the shift register*," as claimed in independent claim 11 (*line 3*);

"*a plurality of pairs of current source circuits, wherein each of the plurality of pairs of current source circuits is configured to receive a set signal and a signal current, and to control an output current value depending on a value of the signal current*," as claimed in independent claim 11 (*lines 4-6*);

"*a changing over circuit electrically connected between the plurality of pairs of current source circuits and a plurality of signal lines*," as claimed in independent claim 11 (*lines 14-15*);

"*wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines*," as claimed in independent claim 11 (*lines 20-22*); and

"*wherein the shift register is configured to output the set signal*," as claimed in independent claim 11 (*line 23*) of the ***Subcombination***.

The ***Combination*** as claimed (*in claims 95 and 96*) does not require:

"*a shift register*," as claimed in independent claim 12 (*line 2*);

"*a latch circuit, electrically connected to the shift register*," as claimed in independent claim 12 (*line 3*);

"*a plurality of pairs of current source circuits, wherein each of the plurality of pairs of current source circuits is configured to receive a set signal and a signal current, and to control an output current value depending on a value of the signal current*," as claimed in independent claim 12 (*lines 4-6*);

"*a changing over circuit electrically connected between the plurality of pairs of current source circuits and a plurality of signal lines*," as claimed in independent claim 12 (*lines 11-12*);

"*wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines*," as claimed in independent claim 12 (*lines 19-21*); and

"*wherein the shift register is configured to output the set signal, and wherein the first and second switches are configured to be controlled based on a same latch pulse*," as claimed in independent claim 12 (*lines 22-24*) of the ***Subcombination***.

The ***Combination*** as claimed (*in claims 95 and 96*) does not require:

"*a plurality of current source circuits, wherein each of the plurality of current source circuits is configured to be supplied with a first current and to supply a second current, and wherein a value of the second current depends on a value of the first current*," as claimed in independent claim 81 (*lines 2-5*);

"*a plurality of signal lines*," as claimed in independent claim 81 (*line 15*); and

"*a selector circuit configured to select one of the plurality of signal lines to which the second current is supplied*," as claimed in independent claim 81 (*lines 16-18*) of the ***Subcombination***.

(2) Furthermore, the ***Subcombination*** has separate utility, such as:

The ***Subcombination*** as claimed (*in claims 11, 12, 81, and 92-94*) can be used without requiring:

"*a display device*," as claimed in independent claim 95 (*line 1*);

"*a first unit comprising: a first current source circuit; a second current source circuit; a first switch configured to select one current source circuit into which a signal current is inputted between the first current source circuit and the second current source circuit; and a second switch configured to select one current source circuit from which a signal current is outputted between the first current source circuit and the second current source circuit*," as claimed in independent claim 95 (*lines 3-11*);

"*a second unit comprising a third current source circuit; a fourth current source circuit; a third switch configured to select one current source circuit into which a signal current is*

inputted between the third current source circuit and the fourth current source circuit; and a fourth switch configured to select one current source circuit from which a signal current is outputted between the third current source circuit and the fourth current source circuit," as claimed in independent claim 95 (*lines 12-20*); and

"*a selector circuit configured to select one signal line into which a signal current is supplied from each of the first unit and the second unit*," as claimed in independent claim 95 (*lines 21-22*) of the ***Combination***.

Since applicant has received an action on the merits for the originally presented (*signal line driver subcombination*) invention, this invention has been constructively elected by original presentation for prosecution on the merits.

Accordingly, ***claims 95 and 96 are withdrawn*** from consideration as being directed to a non-elected (*display device combination*) invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. *Claims 11, 81, 92, and 94* are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 11 recites the limitation "***the plurality of first switch circuits***" (*line 8*). There is insufficient antecedent basis for this limitation in the claim.

6. Claim 11 recites the limitation "***the plurality of pairs of current circuits***" (*line 9*). There is insufficient antecedent basis for this limitation in the claim.

7. Claim 11 recites the limitation "***the plurality of second switch circuits***" (*line 11*). There is insufficient antecedent basis for this limitation in the claim.

8. Claim 81 recites the limitation "***the plurality of first switch circuits***" (*line 9*). There is insufficient antecedent basis for this limitation in the claim.

9. Claim 81 recites the limitation "***the plurality of pairs of current circuits***" (*line 10*). There is insufficient antecedent basis for this limitation in the claim.

10. Claim 81 recites the limitation "***the plurality of second switch circuits***" (*line 12*). There is insufficient antecedent basis for this limitation in the claim.

11. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

12. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. *Claims 11, 12, 81, and 92-94* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Groeneveld et al (US 4,967,140 A)*** in view of ***Koyama et al (US 2001/0048408 A1)***.

Regarding claim 11, ***Groeneveld*** discloses a signal line driver circuit [*e.g., Fig. 4*] comprising:

a shift register [*e.g., Fig. 4: 14*];

a latch circuit [*e.g., Fig. 4: via C1, C2, C3, C4*], electrically connected to the shift register, comprising:

a plurality of pairs of current source circuits [*e.g., Fig. 4: T1C1 + B1, T2C2 + B2, T3C3 + B3, T4C4 + B4*],

wherein each of the plurality of pairs of current source circuits is configured to receive a set signal [*e.g., Fig. 4: signal output by shift register 14*] and a signal current [*e.g., Fig. 4: -ø, I_{ref} via 6*], and

to control an output current value [*e.g., Fig. 4: $I_1+\Delta I_1$, $I_3+\Delta I_3$, $I_4+\Delta I_4$*] depending on a value of the signal current;

a plurality of first switches [*e.g., Fig. 4: S1.1, S2.1, S3.1, S4.1, S1.2, S2.2, S3.2, S4.2*],

wherein each of the plurality of first switch circuits is configured to select one [*e.g., Fig. 4: T1C1, T2C2, T3C3, T4C4*] of one pair of current circuits among the plurality of pairs of current circuits; and

a plurality of second switches [*e.g., Fig. 4: S1.4, S2.4, S3.4, S4.4*],

wherein each of the plurality of second switch circuits is configured to select the other one [*e.g., Fig. 4: B1, B2, B3, B4*] of the one pair of current circuits among the plurality of pairs of current circuits; and

a changing over circuit [*e.g., Fig. 4: S1.3, S2.3, S3.3, S4.3*] electrically connected to the plurality of pairs of current source circuits and a plurality of signal lines [*e.g., Fig. 4: 1, 2, 3*],

wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines, and

wherein the shift register is configured to output the set signal (*see the entire document, including Column 2, Line 30 - Column 6, Line 66*).

Should it be shown that ***Groeneveld*** teaches *a latch circuit and/or a changing over circuit*, as instantly claimed, with insufficient specificity:

Koyama discloses a signal line driver circuit [*Fig. 1*] comprising:

a shift register [*Fig. 1; First - Third Shift Registers*];

a latch circuit [*Fig. 1; LAT Portion*], electrically connected to the shift register, comprising a plurality of pairs of current source circuits [*Fig. 5B*], wherein each of the plurality of pairs of current source circuits includes a transistor having a gate, a source and a drain (*see Pages 5-6; Paragraphs 88-89*); and

a changing over circuit [*Fig. 1; 10a*] electrically connected to the plurality of pairs of current source circuits and a plurality of signal lines [*Fig. 1; S001 - S640*], wherein

each of the plurality of pairs of current source circuits is configured to control an output current value [*Fig. 5B; Output*] depending on a voltage between the gate and the source of the transistor of the pair of current source circuits that is generated by supplying a signal current [*Fig. 5B; Control Signals 1 & 2*] to the transistor while the gate and the drain of the transistor are electrically connected to each other (*see Pages 5-6; Paragraphs 88-89*),

wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines, and

wherein the shift register is configured to output the set signal (*see Page 3; Paragraphs 50-53*).

Groeneveld and ***Koyama*** are analogous art, because they are from the shared inventive field of signal line driver circuitry having current sources, latches and digital to analog converters.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Groeneveld's*** digital-to-analog circuitry [*e.g., Fig. 4*] to form ***Koyama's*** digital-to-analog circuits [*e.g., Fig. 1: DACs*] between ***Koyama's*** latch portion [*e.g., Fig. 4: Lat Portion*] and ***Koyama's*** changing over circuit [*Fig. 1; 10a*], so as to provide a small-sized display signal line driver featuring low voltage DACs within a latch circuit [***Koyama****: Fig. 1: Lat Portion + DACs*].

Regarding claim 92, ***Groeneveld*** discloses each of the plurality of pairs of current source circuits includes

a transistor [*e.g., Fig. 4: T1-T4*] having a gate, a source and a drain and

a capacitor [*e.g., Fig. 4: C1-C4*] having one electrode electrically connected to the source of the transistor and the other electrode electrically connected to the gate of the transistor, and

wherein each of the plurality of pairs of current source circuits is configured to control an output current value depending on a voltage [*e.g., Fig. 4: voltage on the capacitors C1-C4*] between the gate and the source of the transistor of the pair of current source circuits that is generated by supplying a signal current [*e.g., Fig. 4:* I_1, I_2, I_3, $I_4 = I_{ref}$] to the transistor while the gate and the drain of the transistor are electrically connected [*e.g., Fig. 4: via 6, 10, 11, S1.1, S2.1, S3.1, S4.1*] to each other (*e.g., see Column 2, Line 30 - Column 6, Line 66*).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 11; furthermore, ***Groeneveld*** discloses a signal line driver circuit [*e.g., Fig. 4*] comprising:

a shift register [*e.g., Fig. 4: 14*];

a latch circuit [*e.g., Fig. 4: via C1, C2, C3, C4*], electrically connected to the shift register, comprising:

a plurality of pairs of current source circuits [*e.g., Fig. 4: T1C1 + B1, T2C2 + B2, T3C3 + B3, T4C4 + B4*],

wherein each of the plurality of pairs of current source circuits is configured to receive a set signal [*e.g., Fig. 4: signal output by shift register 14*] and a signal current [*e.g., Fig. 4: -ø,* I_{ref} *via 6*], and

to control an output current value [*e.g., Fig. 4:* $I_1+\Delta I_1$, $I_3+\Delta I_3$, $I_4+\Delta I_4$] depending on a value of the signal current;

a first switch [*e.g., Fig. 4: S1.1, S2.1, S3.1, S4.1, S1.2, S2.2, S3.2, S4.2*] provided between the shift register and each of the plurality of pairs of current source circuits; and

a second switch [*e.g., Fig. 4: S1.4, S2.4, S3.4, S4.4*], and

a changing over circuit [*e.g., Fig. 4: S1.3, S2.3, S3.3, S4.3*] electrically connected between the plurality of pairs of current source circuits and a plurality of signal lines [*e.g., Fig. 4: 1, 2, 3*],

wherein the changing over circuit is electrically connected to a particular pair of current source circuits [*e.g., Fig. 4: T1C1 + B1*] through the second switch,

wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines,

wherein the shift register is configured to output the set signal, and

wherein the first and second switches are configured to be controlled based on a same latch pulse [*e.g., Fig. 4: signal pulse output by shift register 14*] (*see the entire document, including Column 2, Line 30 - Column 6, Line 66*).

Regarding claim 93, this claim is rejected by the reasoning applied in rejecting claim 92.

Regarding claim 81, this claim is rejected by the reasoning applied in rejecting claims 11 and 12; furthermore, ***Groeneveld*** discloses a signal line driver circuit [*e.g., Fig. 4*] comprising:

a plurality of current source circuits [*e.g., Fig. 4: T1C1 + B1, T2C2 + B2, T3C3 + B3, T4C4 + B4*],

wherein each of the plurality of current source circuits is configured to be supplied with a first current [*e.g., Fig. 4: -ø, I_{ref} via 6*] and to supply a second current [*e.g., Fig. 4: $I_1+\Delta I_1$, $I_3+\Delta I_3$, $I_4+\Delta I_4$*], and

wherein a value of the second current depends on a value of the first current;

a plurality of first switches [*e.g., Fig. 4: S1.1, S2.1, S3.1, S4.1, S1.2, S2.2, S3.2, S4.2*],

wherein each of the plurality of first switch circuits is configured to select one [*e.g., Fig. 4: T1C1, T2C2, T3C3, T4C4*] of one pair of current circuits among the plurality of pairs of current circuits;

a plurality of second switches [*e.g., Fig. 4: S1.4, S2.4, S3.4, S4.4*],

wherein each of the plurality of second switch circuits is configured to select the other one [*e.g., Fig. 4: B1, B2, B3, B4*] of the one pair of current circuits among the plurality of pairs of current circuits;

a plurality of signal lines [*e.g., Fig. 4: 1, 2, 3*]; and

a selector circuit [*e.g., Fig. 4: S1.3, S2.3, S3.3, S4.3*] configured to select one of the plurality of signal lines to which the second current is supplied (*see the entire document, including Column 2, Line 30 - Column 6, Line 66*).

Regarding claim 94, this claim is rejected by the reasoning applied in rejecting claim 92.

Response to Arguments

16. Applicant's arguments filed on *29 January 2010* have been fully considered but they are not persuasive.

Applicant's arguments with respect to *claims 11, 12, 81, and 92-94* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
30 April 2010